Experiment 10

Field Effect Transistor (FET)

1- Objects of the Experiment:

- Study the drain current - voltage characteristics for n-channel JFET.
- Representing the relationship between drain current, I_D, and gate to source voltage, V_{GS}, for the transistor biased in the saturation region.

2- Principles

The acronym 'FET' stands for **field effect transistor**. It is a three-terminal unipolar solid-state device in which current is controlled by an **electric field.**

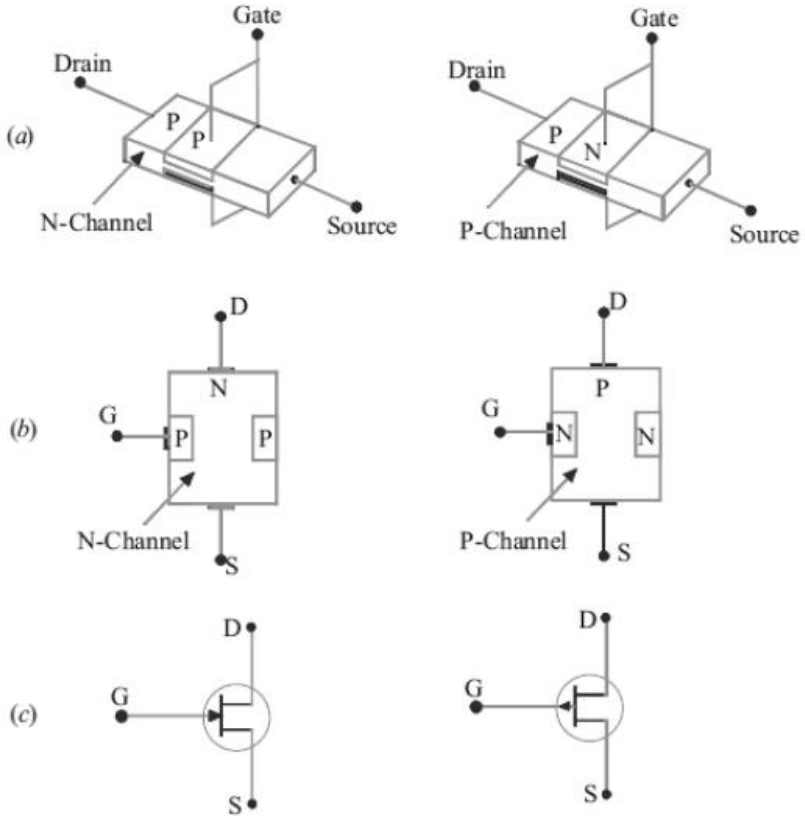

Fig. 1 FET construction

As shown in Fig.1, it can be fabricated with either an N-channel or P-channel though N-channel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of

N-type semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part [Fig.1 (a)]. These junctions form two P-N diodes or gates and the area between these gates is called channel. The two P-regions are internally connected and a single lead is brought out which is called gate terminal. Ohmic contacts (direct electrical connections) are made at the two ends of the bar-one lead is called source terminal S and the other drain terminal D. When potential difference is established between drain and source (V_{DS}), current (I_D) flows along the length of the 'bar' through the channel located between the two P regions. The current consists of only majority carriers which, in the present case, are electrons. P-channel JFET is similar in construction except that it uses P-type bar and two N type junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates.

Following FET notation is worth remembering:

- **Source**: it is the terminal through which majority carriers enter the bar. Since carriers come from it, it is called the source.
- **Drain**: it is the terminal through which majority carriers leave the bar i.e. they are drained out from this terminal. The drain to source voltage, V_{DS}, drives the drain current I_D.
- **Gates**: these are two internally-connected heavily-doped impurity regions which form two P-N junctions. The gate-source voltage VGS reverse biases the gates.
- **Channel**: it is the space between two gates through which majority carriers pass from source-to-drain when V_{DS} is applied.

Schematic symbols for N-channel and P-channel JFET are shown in Fig.1 (c). It must be kept in mind that gate arrow always points to N-type material.

We will consider the following two characteristics:

- **Drain characteristics**: it gives relation between I_D and V_{DS} for different values of V_{GS} (which is called running variable).
- **Transfer characteristics**: It gives relation between I_D and V_{GS} for different values of V_{DS} in the saturation region.

We will analyze these characteristics for an N-channel JFET connected in the common-source mode as shown in Fig. 2.

3- Equipment

1 Power supply unit	727 88
1 resistor 1kΩ / 2W	577 44
1 resistor 47kΩ / 0.5W	577 64
1 potentiometer 10 kΩ / 1W	577 925
1 potentiometer 100 kΩ / 1W	577 96
1 FET transistor BF 244	578 77
3 multimeters	
1 Plug-in board 297X300	72650
1 Set of bridging plugs 19mm	501 48
1 Set of connecting leads	501 532

4- Setup and carrying out the experiment

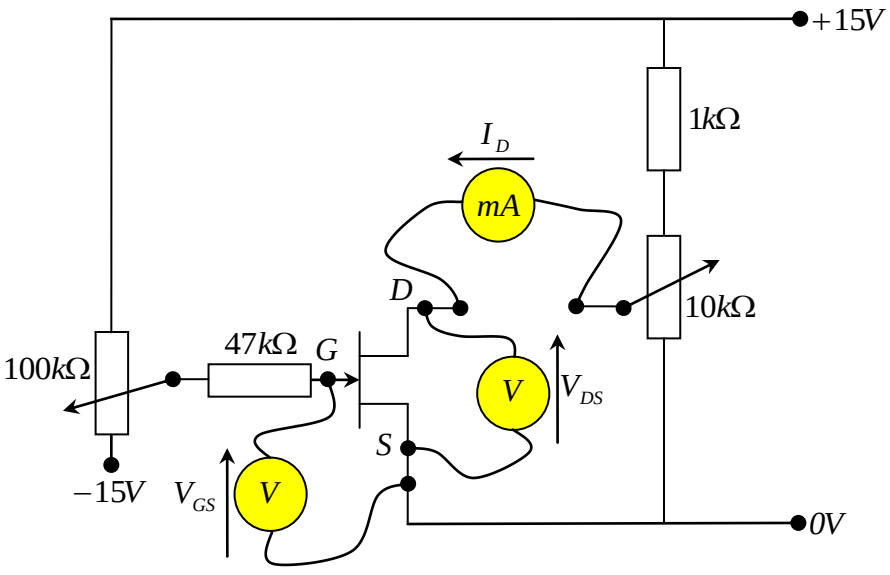

Figure 2.

4-1- Study the drain voltage-current characteristic:

- Assemble the circuit as shown in Figure 2

- Set a gate voltage V_{GS} = -1.3V by using the 100kΩ potentiometer

- Measure the relation between I_D (multimeter) and V_{DS} (multimeter) and enter the values in Table 1.

Table 1

V_{DS} (V)	**I_D (mA)**
0	
0.2	
0.5	
1	
1.5	
2	
2.5	
3	
3.5	
4	
4.5	
5	

-Repeat measuring for different value of V_{GS}=(-1V, -0.6V, -0.3V, 0.0V, 0.2V, 0.4V)

- Prepare a sheet of graph paper for plotting I_D versus V_{DS}. You should make I_D the vertical axis and V_{DS} the horizontal axis. Each axis should be labeled and appropriate units indicated. The graph should have a title.

- Plot your data from Table 1 and draw the graph of $I_D = f(V_{DS})$.

4-2- Representing the relationship between I_D and V_{GS} .

- Directly from the graph fill Table 2 by taking the drain voltage V_{DS} at a fixed value in saturation region

Table 2.

V_{GS} (V)	I_D(mA)
-1.3	
-1.0	
-0.6	
-0.3	
0.0	
0.2	
0.4	

- Prepare a sheet of graph paper for plotting I_D versus V_{GS}. You should make I_D the vertical axis and V_{GS} the horizontal axis. Each axis should be labeled and appropriate units indicated. The graph should have a title.
- Plot your data from Table 1 and draw the graph of $I_D = f(V_{GS})$.

5- Conclusion

Make a general conclusion about the experiments and the results obtained.